REMARKS

In the Office Action mailed August 10, 2004, the Examiner objected to the drawings. Transmitted herewith are proposed drawings with FIG. 6 on the bottom of the page, and the reference 700 duplicated as intended. Reconsideration of the drawings is respectfully requested.

The Examiner objected to the specification because FIG. 8 is not described, and reference 1208 does not appear in the drawings. Amendments to the specification are included herein, and reconsideration of the specification is requested.

In the Office Action, the Examiner rejected claims 1-4, 8-10, and 14 under 35 USC Section 103 as being unpatentable over Yamaguchi et al in view of Tong et al. In view of the following comments, the Examiner's rejection is respectfully traversed, and reconsideration of the claims is requested.

Claim 1 recites, *inter alia*,

> "coding an input data stream into systematic bits and parity bits;
> loading the systematic bits and parity bits into respective systematic and parity block interleavers in a column-wise manner;
> selecting a predefined redundancy; and ..."

Yamaguchi discloses interleaving and then coding. Additionally, Yamaguchi fails to disclose selecting a predefined redundancy. Accordingly, Yamaguchi fails to show or suggest the basic structure of claim 1.

The secondary reference to Tong et al fails to suggest modification of Yamaguchi as suggested by the Examiner. The Examiner in picking an choosing from the references without consideration for what the references themselves fairly teach of one of ordinary skill in that art, making an impermissible hindsight reconstruction of the claimed invention. Accordingly, the Examiner failed to make a *primia facie* case of obviousness.

Claim 8 recites, *inter alia*,

> turbo coding an input data stream into systematic bits and parity bits;
> loading the systematic bits and parity bits into respective systematic and parity block interleavers in a column-wise manner;
> selecting a predetermined redundancy; and

> mapping the bits from the systematic and parity block interleavers into a symbol mapping array in a row-wise manner in accordance with the selected redundancy, wherein the systematic bits are mapped into the upper rows of the array and the parity bits are mapped into the lower rows of the array.

Again, it is respectfully submitted that Yamuguchi teaches away from the claimed method, teaching a different method. Furthermore, there is no motivation in Yamagushi or Tong for Applicants' novel method.

Claim 14 recites, *inter alia*,

> a channel coder operable to code an input data stream into systematic bits and parity bits;
>
> a first interleaver coupled to the channel coder, the first interleaver operable to load the systematic bits and parity bits into respective systematic and parity block interleavers in a column-wise manner;
>
> a redundancy version selector coupled to the first interleaver, the redundancy version selector operable to select a predefined redundancy;
>
> a bit priority mapper coupled to the redundancy version selector, the bit priority mapper operable to map bits from the block interleavers in a row-wise manner in accordance with the selected predefined redundancy.

Neither Yamaguchi nor Tong shows or suggests the novel claimed structure.

Accordingly, it is respectfully submitted that the claims clearly define the invention and are in condition for allowance. A Notice of Allowance is solicited.

Respectfully Submitted
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